# PARSA MIRFASIHI

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## OBJECTIVES

Accomplished Electrical and Computer Engineer with expertise in VLSI and hardware design, specializing in ASIC and FPGA development, RTL design, functional verification, and physical design. Proficient in SystemVerilog, advanced verification methodologies, and industry-standard EDA tools, with strong experience in debugging, optimization, and automation using Python. Seeking opportunities as a Physical Design Engineer, ASIC Design Engineer, FPGA Engineer, Design Verification Engineer, or related roles in digital and VLSI design where I can contribute to semiconductor technologies.

## PROFESSIONAL SKILLS

**Digital & VLSI Design** (ASIC/SoC, RTL, FPGA, RTL-to-GDSII, STA, DFT, Low-Power), **Verification** (SystemVerilog, UVM, Testbenches, Functional Verification), **Physical Design** (PnR, STA, PPA optimization), **Analog & Mixed-Signal** (IC validation, SPICE, PCB, Signal/Power Integrity), **Programming & Automation** (Python, Tcl, Perl, Algorithms, Workflow Automation), **EDA Tools** (**Synopsys**: Design Compiler, PrimeTime, VCS, **Cadence**: Virtuoso, Innovus, Genus).
**Languages & Tools:** SystemVerilog, VHDL, Linux/Unix, Altium
**Measurement Tools:** Teradyne ATE (J750), Oscilloscope, Logic Analyzer, Waveform Generator

## PROFESSIONAL EXPERIENCE

**San Francisco State University - San Francisco, CA** **January 2025 - Present**
**Graduate Student Researcher, Nano-Electronics & Computing Research Lab**
Developed an ML-driven framework to optimize distributed RC network modeling, addressing the tradeoff between speed and accuracy that slows timing closure and design efficiency. The solution delivered faster, more scalable interconnect modeling with **<5% delay error**, significantly improving the accuracy and reliability of timing analysis.

- Integrated Python automation with SPICE to extract propagation delay, slew, and tail behavior under varying resistance, capacitance, and segmentation.
- Implemented a driving-point admittance propagation algorithm to generate reduced-order models tailored to each network.
- Benchmarked reduced models against full RC-tree simulations, consistently achieving less than 5% delay error. Conducted extensive transient and parametric sweeps in HSPICE to validate accuracy and identify cases requiring higher-order representations.

**Industrial Assessment Center (IAC) – San Francisco, CA** **September 2024 – April 2025**
**Energy Engineer – Part time**
funded by the U.S. Department of Energy. Performed comprehensive data analysis and developed detailed engineering and economic reports outlining energy-saving recommendations. Identified and proposed solutions in Energy Conservation, Waste Minimization, Water Conservation, and Productivity Improvement.

- Led an energy audit at Air Monitor, recommending a fluorescent-to-LED retrofit that delivered an estimated 33,877 kWh/year in energy savings and $13,799/year in cost savings, with a simple payback period of 0.9 years.
- Conducted additional audits, including Sierra Nevada Brewery, where actionable recommendations improved operational efficiency and reduced energy consumption.

**San Francisco State University, CA** **September 2024 - May 2025**

**Teaching Assistant – Part time**

Digital Design System/Laboratory, Control Systems, Computer Systems, Linear System Analysis, Operational Amplifier System Design, Communication Systems

## RELEVANT PROJECTS

**ASIC Implementation of Motion Estimator in 14nm FinFET Technology**

Designed and implemented a motion estimator for video compression using the Block-Matching Algorithm with a 16×16 reference block and 32×32 search block, achieving a high-throughput pipelined architecture. Completed the full RTL-to-GDSII flow with successful sign-off, including Verilog module development (Processing Elements, Comparator, Controller), synthesis, static timing analysis, and back-end physical design. Performed area and power optimization, ECO-based hold violation correction, and physical verification (DRC), reinforcing expertise in ASIC design, physical implementation, and advanced node technology.

**Custom SRAM Design in 14nm CMOS Technology**

Designed a 16×18 SRAM architecture in Synopsys Custom Compiler, optimized for area, access time, and power efficiency. Implemented and verified precharge unit, write driver, sense amplifier, address decoder, and SRAM cell array while ensuring robust read/write functionality and signal integrity. Conducted functional verification and power characterization using structured read/write test sequences in Custom Compiler and WaveView, and validated design integrity by clearing DRC and LVS checks for compliance with advanced-node rules.

**DFT-Oriented PCB for Power and Signal Integrity Validation of Mixed-Signal SoC using Teradyne J750**

Designed a custom PCB to support DFT validation of a mixed-signal SoC with emphasis on PDN stability, clock distribution, and high-speed signal integrity. Incorporated decoupling capacitor networks, controlled impedance traces, analog test access points, and boundary-scan hooks to monitor IR drop, voltage ripple, jitter, and crosstalk. Leveraged the Teradyne J750 ATE to apply functional/parametric test vectors, measure delay and noise margins, and characterize analog/digital interactions under stress conditions, enhancing expertise in mixed-signal PCB design, DFT methodologies, and ATE-based validation.

**Teradyne J750 Semiconductor Test System Training & Setup**

Collaborated with Teradyne experts during installation of the J750 semiconductor test system at SFSU's Nano Electronics & Computing Research Lab, gaining hands-on experience in setup, calibration, and device testing. Trained in test procedures, hardware/software integration, and IG-XL software development; assisted with calibration; developed scan, ADC, and DAC tests; and authored a technical report documenting system specifications, capabilities, and setup as a reference for future lab users.

## EDUCATION

**San Francisco State University, San Francisco, CA** **January 2024 - May 2026 (Expected)**

Master of Science in Electrical and Computer Engineering - GPA: 4.00/4.00

**Iran University of Science and Technology, Tehran, Iran** **September 2017-May 2022**

Bachelor of Science in Electrical Engineering - GPA: 3.7 / 4.00

## PUBLICATIONS

**Designing and implementing a real-time intelligent system for object identification and classification**

This work presents a real-time object detection and classification system for autonomous vehicles using TensorFlow on an NVIDIA Quadro 1000P GPU. The system achieved 21 FPS with SSD + InceptionV2 and 88% mAP with Mask R-CNN on the MS COCO dataset. **19 June 2022, Tehran, Iran**